

Agilent Technologies 16900 Series Modules

Data Sheet

The Agilent 16900 Series logic analysis modules offer the speed, features, and usability your digital development team needs to quickly debug, validate, and optimize your digital system—at a price that fits your budget.

16900 Series timing and state modules give you the power to:

- Accurately measure precise timing relationships using 4 GHz (250 ps) timing zoom with 64 K depth.
- Extend the measurement window with precision when signals transition less frequently using transitional timing.
- Find anomalies separated in time with deep memory depths.
- Buy what you need today and upgrade in the future.
 16900 Series timing/state modules come with independent upgrades for memory depth and state speed.
- Sample high-speed synchronous buses accurately and confidently using eye finder. Eye finder automatically adjusts setup and hold for your highest confidence in measurements on high-speed buses.

- Track problems from symptom to root cause across several measurement modes by viewing time-correlated data in waveform/chart, listing, inverse assembly, source code, or compare display.
- Set up triggers quickly and confidently with intuitive simple, quick, and advanced triggering. This capability combines new trigger functionality with an intuitive user interface.
- The Agilent 16900 Series modules are compatible with the industry's widest range of probing accessories with capacitive loading down to 0.7 pF.
- Monitor and correlate multiple buses using a single module with split analyzer capability. This provides single and multi-bus support using a single module (timing, state, timing/state or state/state configurations).



Agilent 16900 Series Logic Analysis Modules







| Agilent Model Number | Support for the Industry's Fastest Buses 16950A | High-Performance 16910A | High-Performance 16911A |
|---|---|--|--|
| Channels per module | 68 | 102 | 68 |
| Maximum channels on single time base | 340 | 510 | 340 |
| Timing Mode | | | |
| High-speed timing zoom [1] | 4 GHz (250 ps) with 64 K depth | 4 GHz (250 ps) with 64 K depth | 4 GHz (250 ps) with 64 K depth |
| Maximum timing sample rate: half channel mode | 1.2 GHz (833 ps) | 1.0 GHz (1 ns) | 1.0 GHz (1 ns) |
| Maximum timing sample rate: full channel mode | 600 MHz (1.67 ns) | 500 MHz (2.0 ns) | 500 MHz (2.0 ns) |
| Transitional timing | 600 MHz (1.67 ns) | 500 MHz (2.0 ns) | 500 MHz (2.0 ns) |
| State Mode | | | |
| Maximum state clock rate | 600 MHz | 450 MHz with option 500, 250 MHz with option 250 | 450 MHz with option 500, 250 MHz with option 250 |
| Maximum state data rate | 800 Mb/s | 500 Mb/s with option 500, 250 Mb/s with option 250 | 500 Mb/s with option 500, 250 Mb/s with option 250 |
| Setup/hold window Adjustment resolution | 1 ns (600 ps typical), 80 ps typical | 80 ps typical | 80 ps typical |
| State clock, data rate (upgradeable) | No | Yes (Agilent E5865A) | Yes (Agilent E5866A) |
| Eye finder capability | Yes | Yes | Yes |
| Memory Depth [2] | | | |
| 64 M 32 M 16 M 4 M 1 M 256 K | Option 064 Option 032 Option 016 Option 004 Option 001 Option 256 | Option 032 Option 016 Option 004 Option 001 Option 256 | Option 032 Option 016 Option 004 Option 001 Option 256 |
| Memory depth (upgradeable) | Yes (Agilent E5875A) | Yes (Agilent E5865A) | Yes (Agilent E5866A) |
| Other | | | |
| Supported signal types | Single-ended and differential | Single-ended | Single-ended |
| Eye scan capability | Yes, in future software release | No | No |
| Probe compatibility [3] | 90-pin cable connector | 40-pin cable connector | 40-pin cable connector |
| Voltage threshold | -3 V to 5 V (10 mV increments) | -5 V to 5 V (10 mV increments) | -5 V to 5 V (10 mV increments) |

 $[\]label{eq:continuous} \textbf{[1]} \ \ \textbf{All channels, all the time, simultaneous state and timing through same probe.}$

^[2] Specify desired memory depth using available options.

^[3] Probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer and the device under test.

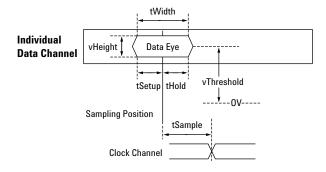
| Module Channel Counts | State Analysis 16910A | State Analysis 16911A | Timing Analysis 16910A | Timing Analysis 16911A |
|-----------------------|--------------------------|--------------------------|---------------------------|---------------------------|
| 1-card module | 98 data + 4 clocks | 64 data + 4 clocks | 102 | 68 |
| 2-card module | 200 data + 4 clocks | 132 data + 4 clocks | 204 | 136 |
| 3-card module | 302 data + 4 clocks | 200 data + 4 clocks | 306 | 204 |
| 4-card module | 404 data + 4 clocks | 268 data + 4 clocks | 408 | 272 |
| 5-card module | 506 data + 4 clocks | 336 data + 4 clocks | 510 | 340 |

Probes

A probe must be used to connect the logic analyzer to your target system. Probes are ordered separately from the logic analysis module. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number in this help system or at **www.agilent.com** or *Probing Solutions for Agilent Technologies Logic Analyzers* Product Overview, publication number 5968-4632E.

Timing Zoom

| Timing analysis sample rate | 4 GHz | |
|-----------------------------|--|--|
| Time interval accuracy | | |
| Within a pod pair | \pm (1.0 ns + 0.01% of time interval reading) | |
| Between pod pairs | \pm (1.75 ns + 0.01% of time interval reading) | |
| Memory depth | 64 K samples | |
| Trigger position | Start, center, end, or user-defined | |
| Minimum data pulse width | 1 ns | |



| State (Synchronous) Analysis Mode | Option 250 | Option 500 |
|--|---|---|
| tWidth* [1] | 1.5 ns | 1.5 ns |
| tSetup | 0.5 tWidth | 0.5 tWidth |
| tHold | 0.5 tWidth | 0.5 tWidth |
| tSample range [2] | -3.2 ns to +3.2 ns | -3.2 ns to +3.2 ns |
| tSample adjustment resolution | 80 ps typical | 80 ps typical |
| Maximum state data rate on each channel | 250 Mb/s | 500 Mb/s |
| Maximum channels on a single time base and trigger [4] | 16910A: 510 – (number of clocks) 16911A: 340 – (number of clocks) | 16910A: 510 – (number of clocks) 16911A: 340 – (number of clocks) |
| Memory depth [4] | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples |
| Number of independent analyzers [5] | 2 | 1 |
| Number of clocks [6] | 4 | 1 |
| Number of clock qualifiers [6] | 4 | N/A |
| Minimum time between active clock edges* [7] | 4.0 ns | 2.0 ns |
| Minimum master to slave clock time | 1 ns | N/A |
| Minimum slave to master clock time | 1 ns | N/A |
| Minimum slave to slave clock time | 4.0 ns | N/A |

^{*} Items marked with an asterisk (*) are specifications. All others are characteristics.

[&]quot;Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

^[1] Minimum eye width in system under test.

^[2] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

^[3] Use of eye finder is recommended in 450 MHz and 500 Mb/s state mode.

^[4] In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full. One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.

 $^{[5] \ \} Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.$

^[6] In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

^[7] Tested with input signal Vh = ± 1.3 V, VI = ± 0.7 V, threshold = ± 1.0 V, tr/tf = ± 1.0 ps ± 30 ps (± 1.0 ps ± 3.0 ps ($\pm 3.$

| State (Synchronous) Analysis Mode | Option 250 | Option 500 |
|---|---|--|
| Minimum state clock pulse width Single edge Multiple edge | 1.0 ns 1.0 ns | 1.0 ns 2.0 ns |
| Clock qualifier setup time | 500 ps | N/A |
| Clock qualifier hold time | 0 | N/A |
| Time tag resolution | 2 ns | 1.5 ns |
| Maximum time count between stored states | 32 days | 32 days |
| Maximum trigger sequence speed | 250 MHz | 500 MHz |
| Maximum trigger sequence levels | 16 | 16 |
| Trigger sequence level branching | Arbitrary 4-way if/then/else | 2-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags | 14 patterns evaluated as =, =/, >, ≥, <, ≤ 7 double-bounded ranges evaluated as in range, not in range 1 occurrence counter per sequence level 4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To Trigger, send e-mail, and fill memory Trigger and Go To Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear | Go To Trigger and fill memory |
| Store qualification | Default (global) and per sequence level | Default (global) |
| Maximum global counter | 2E+24 | N/A |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum pattern width | 128 bits | 128 bits |
| Maximum range width | 32 bits | 32 bits |
| Timers range | 60 ns to 2199 seconds | N/A |
| Timer resolution | 2 ns | N/A |
| Timer accuracy | ± (5 ns +0.01%) | N/A |
| Timer reset latency | 60 ns | N/A |

| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing [8] |
|--|---|--|
| Sample rate on all channels | 500 MHz | 500 MHz |
| Sample rate in half channel mode | 1000 MHz | N/A |
| Number of channels | 16910A: 102 x (number of modules) | 16910A: For sample rates < 500 MHz: 102 x (number of modules) For 500 MHz sample rate: 102 x (number of modules) – 34 |
| | 16911A: 68 x (number of modules) | 16911A: For sample rates < 500 MHz: 68 x (number of modules) For 500 MHz sample rate: 68 x (number of modules) – 34 |
| Maximum channels on a single time base and trigger | 16910A: 510 16911A: 340 | 16910A: 510 16911A: 340 |
| Number of independent analyzers [5] | 2 | 2 |
| Sample period (half channel) | 1.0 ns | N/A |
| Minimum sample period (full channel) | 2.0 ns | 2.0 ns |
| Minimum data pulse width | 1 sample period + 1.0 ns | 1 sample period + 1.0 ns |
| Time interval accuracy | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) |
| Memory depth in full channel mode | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples |
| Memory depth in half channel mode | Option 256: 512 K samples Option 001: 2 M samples Option 004: 8 M samples Option 016: 32 M samples Option 032: 64 M samples | N/A |
| Maximum trigger sequence speed | 250 MHz | 250 MHz |
| Maximum trigger sequence levels | 16 | 16 |

 $^{[5] \ \} Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.$

^[8] Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing |
|-------------------------------------|---|---|
| Trigger sequence level branching | Arbitrary 4-way if/then/else | Arbitrary 4-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags | 15 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To Trigger, send e-mail, and fill memory Trigger and Go To Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear | Go To Trigger, send e-mail, and fill memory Trigger and Go To Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear |
| Maximum global counter | 2E+24 | 2E+24 |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum range width | 32 bits | 32 bits |
| Maximum pattern width | 128 bits | 128 bits |
| Timer value range | 60 ns to 2199 seconds | 60 ns to 2199 seconds |
| Timer resolution | 2 ns | 2 ns |
| Timer accuracy | ± (5 ns +0.01%) | ± (5 ns +0.01%) |
| Greater than duration | 4.0 ns to 67 ms in 4.0 ns increments | 4.0 ns to 67 ms in 4.0 ns increments |
| Less than duration | 8.0 ns to 67 ms in 4.0 ns increments | 8.0 ns to 67 ms in 4.0 ns increments |
| Timer reset latency | 60 ns | 60 ns |
| | | |

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only

Operating Environment

| Temperature (except flexible disk media) | 0 to 40 °C (+32 to +104 °F) when operating in a 16900A or 16902A mainframe. 0 to 50 °C (+32 to +122 °F) when operating in a 16903A mainframe. |
|--|---|
| Humidity | 0 to 80% relative humidity at 40 °C (+104 °F). Reliability is enhanced when operating within the range 20% to 80% non-condensing. |
| Altitude | 0 to 3000 m (10,000 ft) |
| Vibration | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms |

Non-Operating Environment

| Temperature | -40 to $+75$ °C (-40 to $+167$ °F). Protect the instrument from temperature extremes which cause condensation on the instrument. |
|--------------------------------|--|
| Humidity | 0 to 90% at 65 °C (149 °F) |
| Altitude | 0 to 15,300 m (50,000 ft) |
| Vibration (in shipping carton) | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |

 $See\ individual\ probe\ Specifications\ and\ Characteristics\ for\ probe\ environmental\ characteristics.$

| Module Channel Counts | State Analysis | Timing Analysis | |
|------------------------------|---------------------|-----------------|--|
| 1-card module | 64 data + 4 clocks | 68 | |
| 2-card module | 132 data + 4 clocks | 136 | |
| 3-card module | 200 data + 4 clocks | 204 | |
| 4-card module | 268 data + 4 clocks | 272 | |
| 5-card module | 336 data + 4 clocks | 340 | |

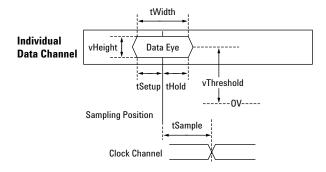
Probes

A probe must be used to connect the logic analyzer to your target system. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number in this help system or at **www.agilent.com**.

Timing Zoom

| Timing analysis sample rate | 4 GHz | |
|-----------------------------|--|--|
| Time interval accuracy | | |
| Within a pod pair | \pm (1.0 ns + 0.01% of time interval reading) | |
| Between pod pairs | \pm (1.75 ns + 0.01% of time interval reading) | |
| Memory depth | 64 K samples | |
| Trigger position | Start, center, end, or user-defined | |
| Minimum data pulse width | 750 ps | |

State (Synchronous) Analysis Mode



| State (Synchronous) Analysis Mode | 300 Mb/s State Mode | 600 Mb/s State Mode |
|--|--|--|
| tWidth* [1, 2] | 1 ns*, 600 ps typical | 1 ns*, 600 ps typical |
| tSetup | 0.5 tWidth | 0.5 tWidth |
| tHold | 0.5 tWidth | 0.5 tWidth |
| tSample range [3] | –4 ns to +4 ns | –4 ns to +4 ns |
| tSample adjustment resolution | 80 ps typical | 80 ps typical |
| tSample accuracy, manual adjustment | ± 300 ps | ± 300 ps [4] |
| Maximum state data rate on each channel | 300 Mb/s | 800 Mb/s |
| Maximum channels on a single time base and trigger [5] | 340 – (number of clocks) | 306 – (1 clock) |
| Memory depth [5] | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples |
| Number of independent analyzers [6] | 2 | 1 |
| Number of clocks [7] | 4 | 1 |
| Number of clock qualifiers [7] | 4 | N/A |
| Minimum time between active clock edges* [8] | 3.33 ns | 1.67 ns |
| Minimum master to slave clock time | 1 ns | N/A |
| Minimum slave to master clock time | 1 ns | N/A |
| Minimum slave to slave clock time | 3.33 ns | N/A |

^{*} Items marked with an asterisk (*) are specifications. All others are characteristics.

[&]quot;Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

^[1] Minimum eye width in system under test.

^[2] Your choice of probe can limit system bandwidth. Choose a probe rated at 600 Mb/s or greater to maintain system bandwidth.

^[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

^[4] Use of eye finder is recommended in 600 Mb/s state mode.

^[5] In 300 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full. One pod pair (34 channels) must remain unassigned for time tags in 600 Mb/s state mode.

^[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.

^[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

^[8] Tested with input signal Vh = ± 1.125 V, VI = ± 0.875 V = 1 V/ns, threshold = ± 1.0 V, tr/tf = ± 1.0 ps ± 3.0 ps (± 1.0

| State (Synchronous) Analysis Mode | 300 Mb/s State Mode | 600 Mb/s State Mode | |
|---|---|--|--|
| Minimum state clock pulse width Single edge Multiple edge | 1.0 ns 1.0 ns | 500 ps 1.67 ns | |
| Clock qualifier setup time | 500 ps | N/A | |
| Clock qualifier hold time | 0 | N/A | |
| Time tag resolution | 2 ns | 1.5 ns | |
| Maximum time count between stored states | 32 days | 32 days | |
| Maximum trigger sequence speed | 300 MHz | 600 MHz | |
| Maximum trigger sequence levels | 16 16 | | |
| Trigger sequence level branching | Arbitrary 4-way if/then/else 2-way if/then/else | | |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined | |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags | 14 patterns evaluated as =, =/, >, ≥, <, ≤ 7 double-bounded ranges evaluated as in range, not in range 1 occurrence counter per sequence level 4 flags | |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations | |
| Trigger actions | Go To Trigger, send e-mail, and fill memory Trigger and Go To Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear | nd Go To on't store sample off default storing art/stop/pause/resume ounter increment/decrement/reset nce counter reset | |
| Store qualification | Default (global) and per sequence level | Default (global) | |
| Maximum global counter | 2E+24 | N/A | |
| Maximum occurrence counter | 2E+24 | 2E+24 | |
| Maximum pattern width | 128 bits | 128 bits | |
| Maximum range width | 32 bits | 32 bits | |
| Timers range | 50 ns to 2199 seconds N/A | | |
| Timer resolution | 2 ns N/A | | |
| Timer accuracy | ± (5 ns +0.01%) | N/A | |
| Timer reset latency | 50 ns | N/A | |
| | | | |

| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing [9] |
|--|---|--|
| Sample rate on all channels | 600 MHz | 600 MHz |
| Sample rate in half channel mode | 1200 MHz | N/A |
| Number of channels | 68 x (number of modules) | For sample rates < 600 MHz: 68 x (number of modules). For 600 MHz sample rate: 68 x (number of modules) — 34 |
| Maximum channels on a single time base and trigger | 340 | 340 |
| Number of independent analyzers [6] | 2 | 2 |
| Sample period (half channel) | 833 ps | N/A |
| Minimum sample period (full channel) | 1.67 ns | 1.67 ns |
| Minimum data pulse width | 1 sample period + 500 ps | 1 sample period + 500 ps |
| Time interval accuracy | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) |
| Memory depth in full channel mode | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples | Option 256: 256 K samples Option 001: 1 M samples Option 004: 4 M samples Option 016: 16 M samples Option 032: 32 M samples Option 064: 64 M samples |
| Memory depth in half channel mode | Option 256: 512 K samples Option 001: 2 M samples Option 004: 8 M samples Option 016: 32 M samples Option 032: 64 M samples Option 064: 128 M samples | N/A |
| Maximum trigger sequence speed | 300 MHz | 300 MHz |
| Maximum trigger sequence levels | 16 | 16 |

^[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[9] Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing |
|-------------------------------------|---|---|
| Trigger sequence level branching | Arbitrary 4-way if/then/else | Arbitrary 4-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags | 15 patterns evaluated as =, =/, >, ≥, <, ≤ 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To Trigger, send e-mail, and fill memory Trigger and Go To Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear | Go To Trigger, send e-mail, and fill memory Trigger and Go To Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear |
| Maximum global counter | 2E+24 | 2E+24 |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum pattern/range width | 32 bits | 32 bits |
| Maximum pattern width | 128 bits | 128 bits |
| Timer value range | 50 ns to 2199 seconds | 50 ns to 2199 seconds |
| Timer resolution | 2 ns | 2 ns |
| Timer accuracy | ± (5 ns +0.01%) | ± (5 ns +0.01%) |
| Greater than duration | 3.33 ns to 55 ms in 3.3 ns increments | 3.33 ns to 55 ms in 3.3 ns increments |
| Less than duration | 6.67 ns to 55 ms in 3.3 ns increments | 6.67 ns to 55 ms in 3.3 ns increments |
| Timer reset latency | 50 ns | 50 ns |
| | | |

Eye Scan Mode

| Equivalent rise time | 150 ps |
|--|------------------------------------|
| Equivalent bandwidth [10] | 2.33 GHz |
| Sample position range relative to clock | –5 ns to +5 ns |
| Sample (time) position resolution | 10 ps |
| Sample (time) position accuracy | ± (50 ps + 0.01 x sample position) |
| Number of channels | 68 x (number of modules) — 1 |
| Input dynamic range | -3.0 Vdc to +5.0 Vdc |
| Threshold range | -3.0 Vdc to +5.0 Vdc |
| Threshold resolution | 1 mV |
| Threshold accuracy | ± (30 mV + 2% of setting) |
| Minimum detectable pulse width at minimum signal amplitude | 600 ps |
| Jitter | 40 ps RMS |
| Noise floor | 40 mV p-p |
| Channel-to-channel skew, maximum between any two channels | 100 ps |
| | |

Power Requirements

All necessary power is supplied by the backplane connector of the logic analysis system mainframe.

Environmental Characteristics

Indoor use only

[10] Calculated from rise time.

Operating Environment

| Temperature (except flexible disk media) | 0 to 40 °C (+32 to +104 °F) when operating in a 16900A or 16902A mainframe. 0 to 50 °C (+32 to +122 °F) when operating in a 16903A mainframe. |
|--|--|
| Humidity | 0 to 80% relative humidity at 40 °C (+104 °F). Reliability is enhanced when operating within the range 20% to 80% non-condensing. |
| Altitude | 0 to 3000 m (10,000 ft) |
| Vibration | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms |

Non-Operating Environment

| Temperature | –40 to +75 °C (–40 to +167 °F). Protect the instrument from temperature extremes which cause condensation on the instrument. | |
|--------------------------------|---|--|
| Humidity | 0 to 90% at 65 °C (149 °F) | |
| Altitude | 0 to 15,300 m (50,000 ft) | |
| Vibration (in shipping carton) | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis | |

See individual probe Specifications and Characteristics for probe environmental characteristics.

The 16900 Series logic analysis system also supports the following 16700 Series logic analysis modules.

Pattern Generation Module

16720A (in future software release)

State/Timing Modules

16740A, 16741A, 16742A 16750A/B, 16751A/B, 16752A/B 16753A, 16754A, 16755A, 16756A

Related Literature

| Publication Title | Publication Type | Publication Number |
|---|---------------------|---------------------------|
| Agilent Technologies 16900 Series Logic Analysis Systems | Color Brochure | 5989-0420EN |
| Agilent Technologies 16900 Series Logic Analysis Systems | Data Sheet | 5989-0421EN |
| Agilent Technologies FPGA Dynamic Probe | Data Sheet | 5989-0423EN |
| Probing Solutions for Agilent Technologies Logic Analyzers | Product Overview | 5968-4632E |
| Processor and Bus Support for Agilent Technologies Logic Analyzers | Configuration Guide | 5966-4365E |

Agilent Technologies' Test and Measurement Support, Services, and Assistance

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Our Promise

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